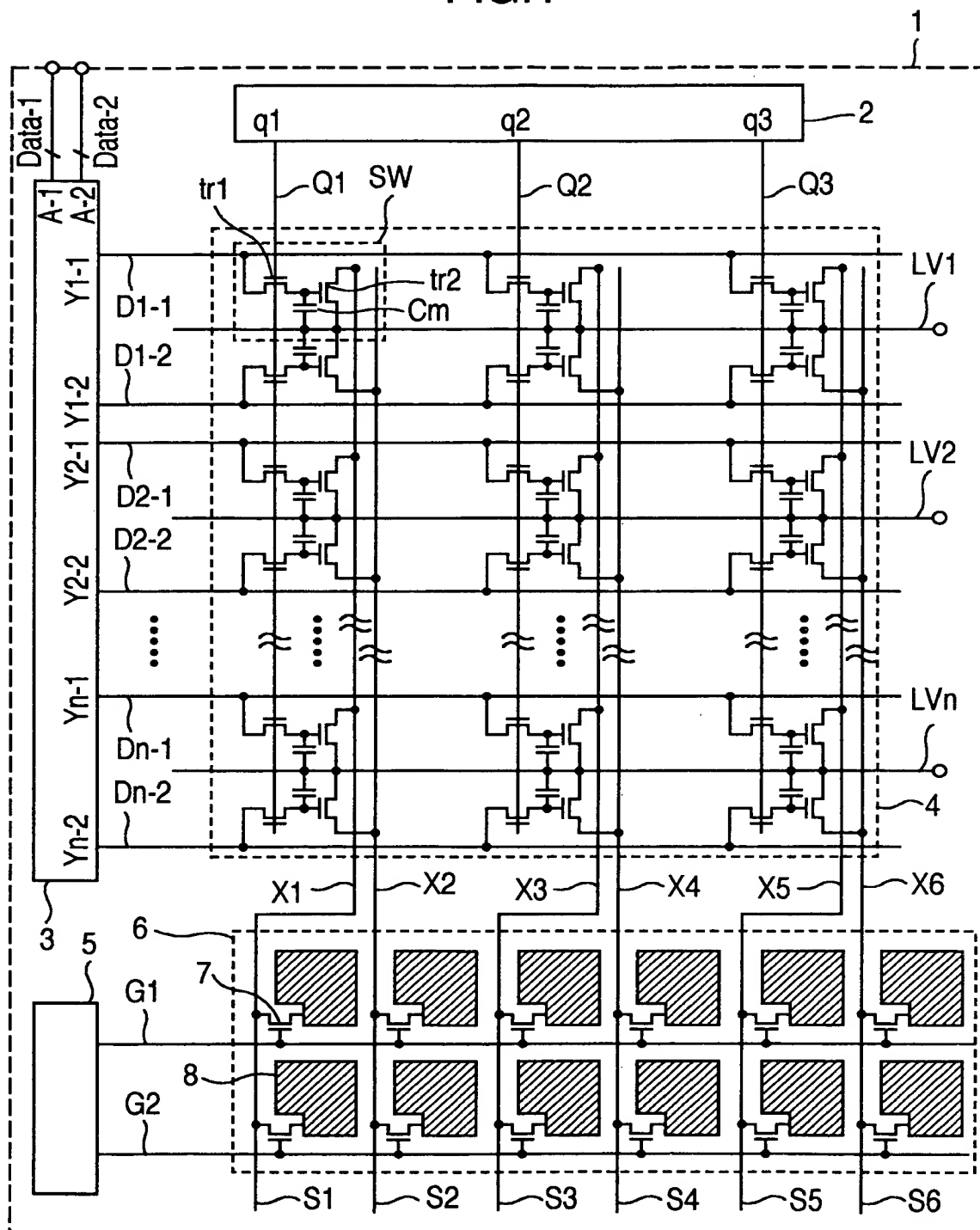


FIG. 1



1 : INSULATING SUBSTRATE
 2 : SHIFT REGISTER
 3 : DECODER
 4 : DA CONVERTER
 5 : SCANNING CIRCUIT

6 : DISPLAY REGION
 7 : PIXEL TFT
 8 : PIXEL
 SW : SWITCH CIRCUIT

FIG.2

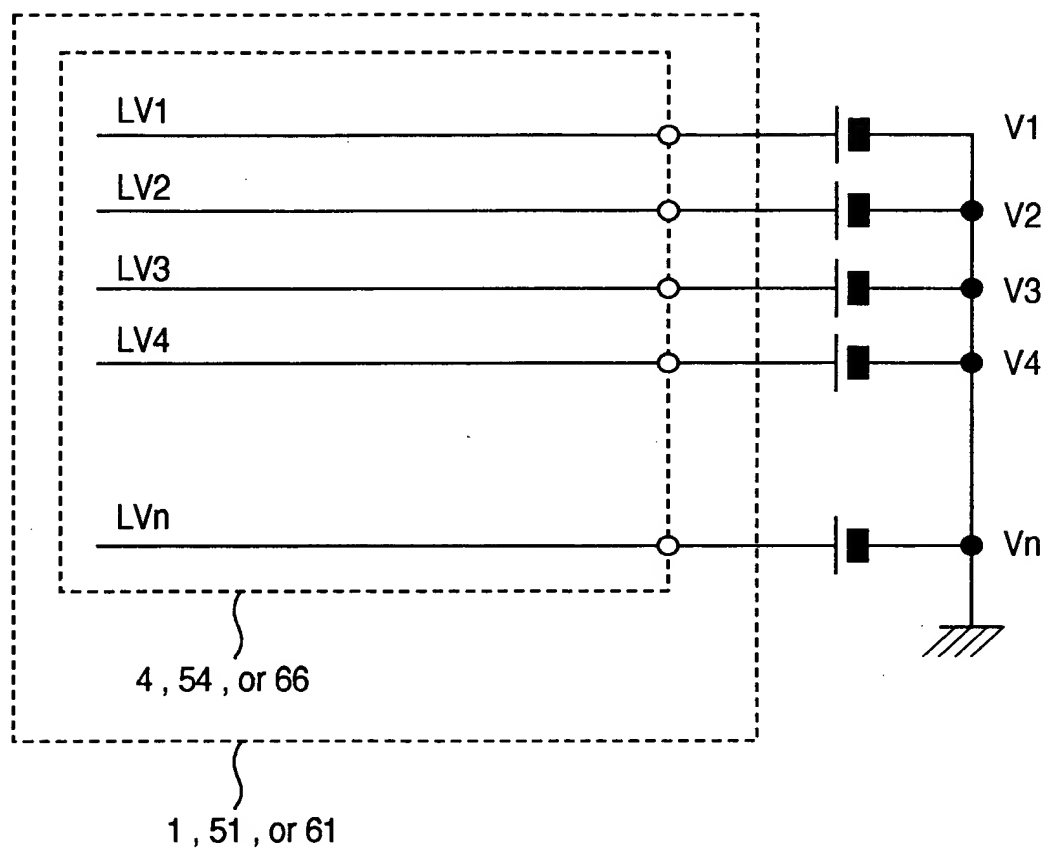


FIG.3

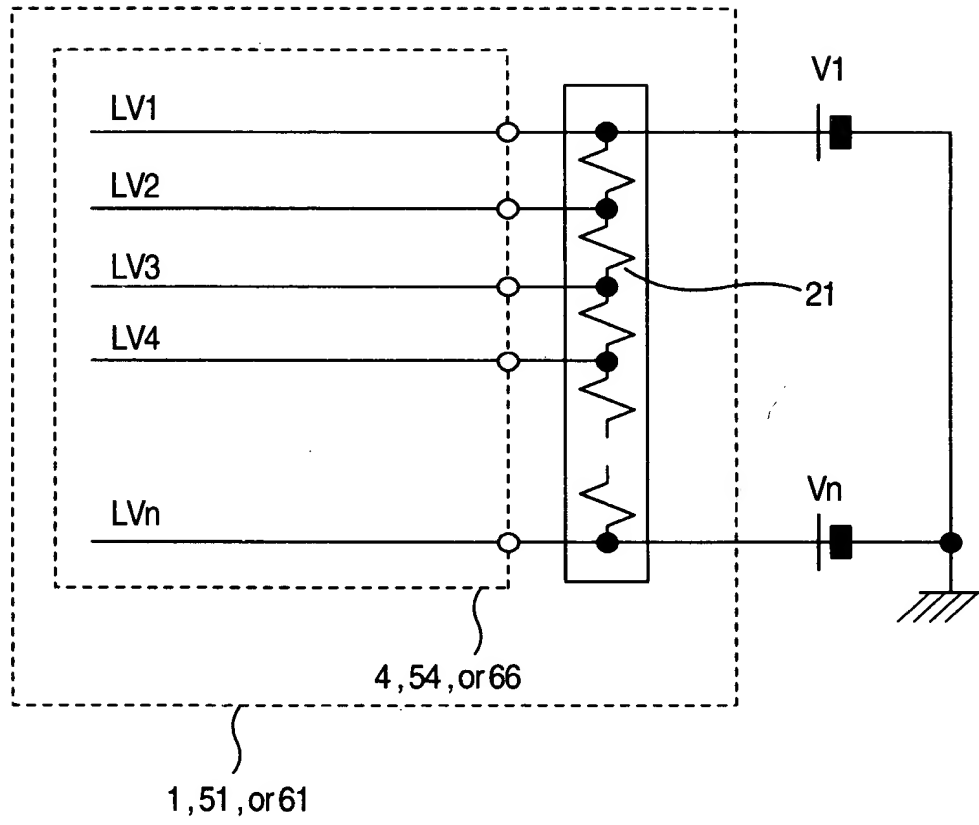


FIG. 3

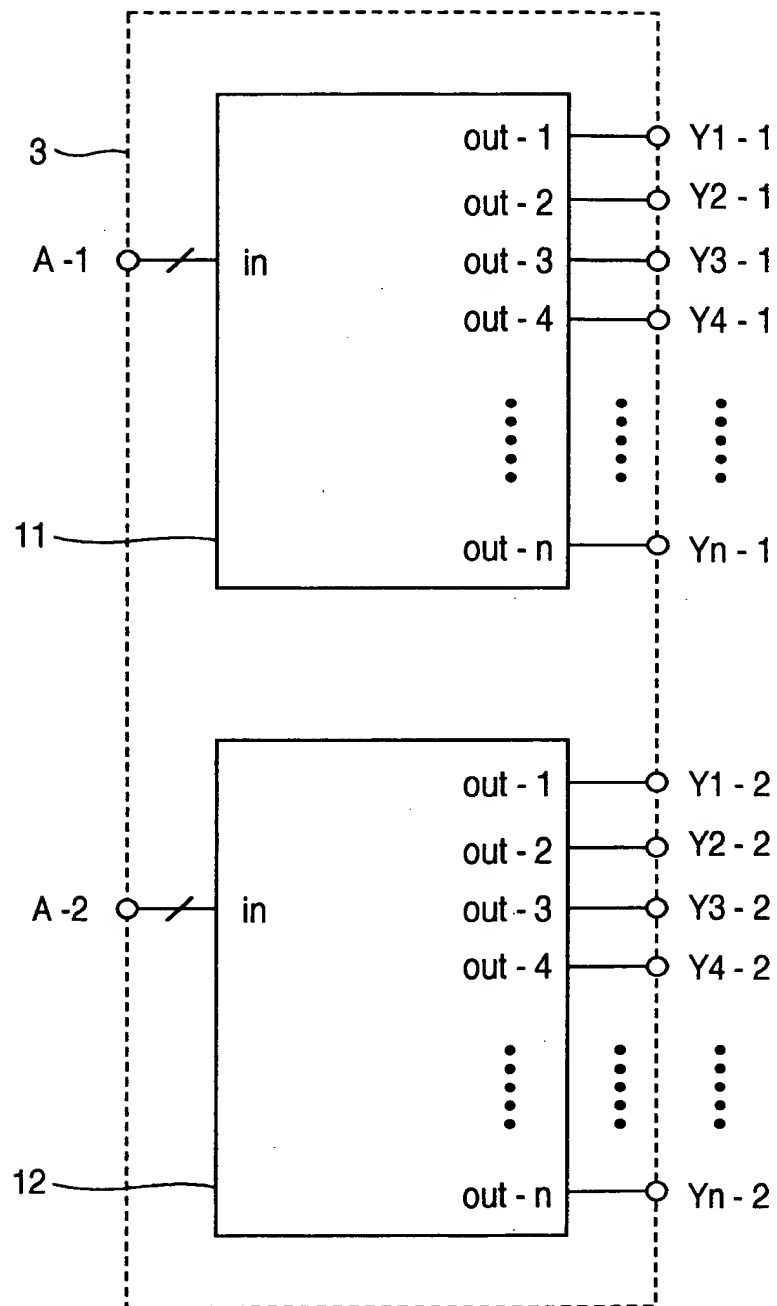


FIG.6

in	out - 1	out - 2	out - 3	out - 4	out - 5	...	out - n
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
...
n	0	0	0	0	0	1

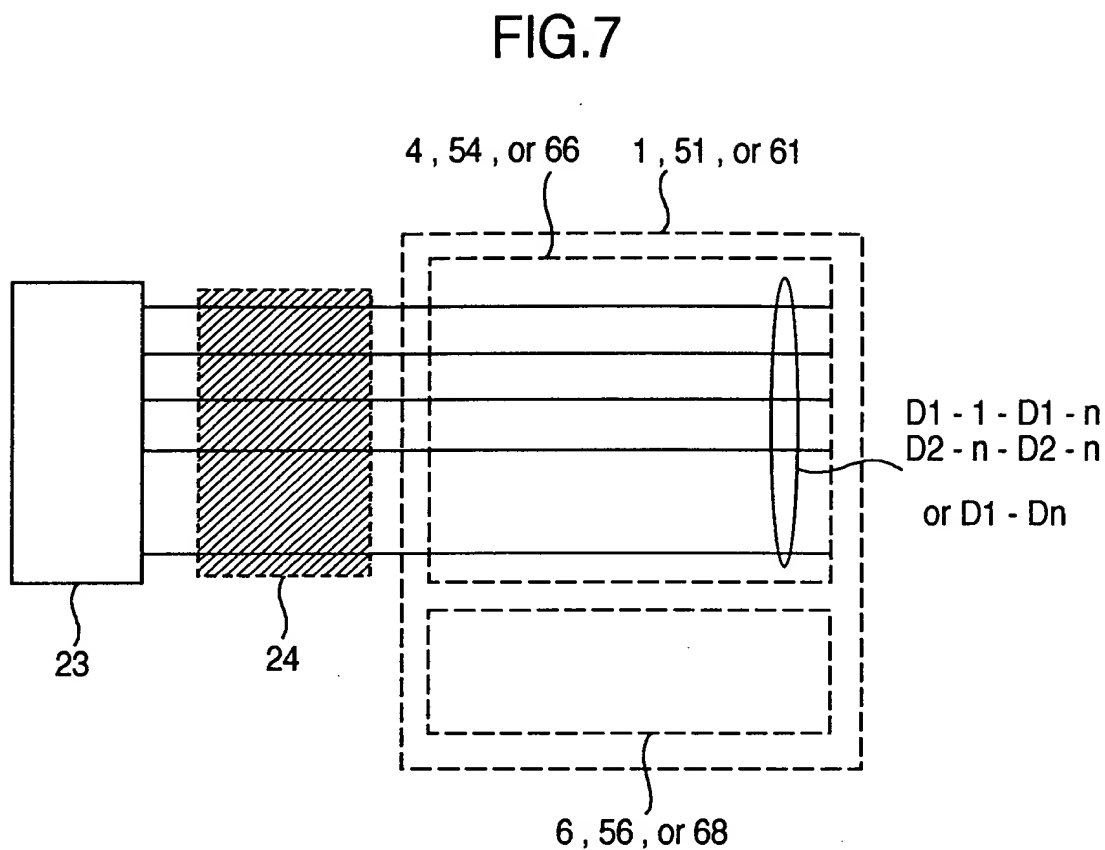


FIG. 8

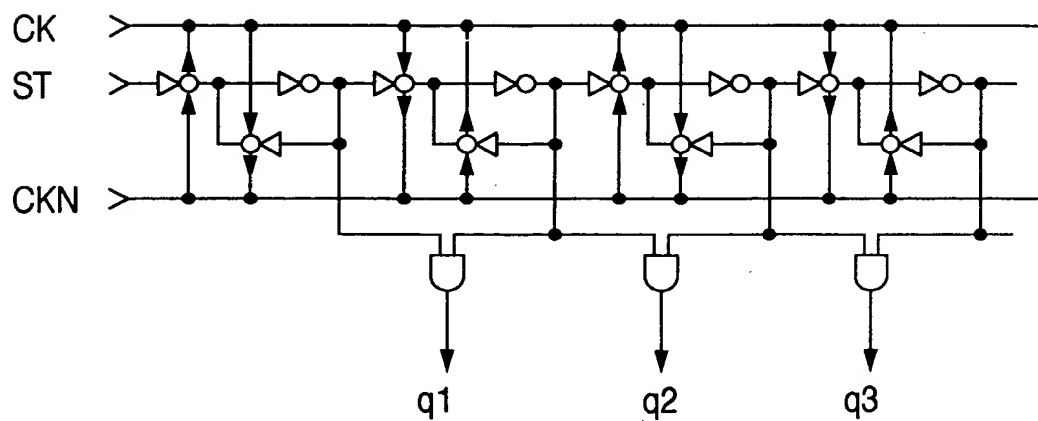


FIG.9A

INVERTER

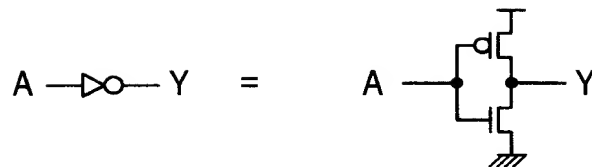


FIG.9B

CLOCKED INVERTER

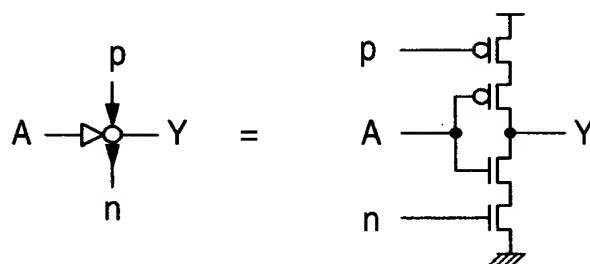


FIG.9C

AND GATE

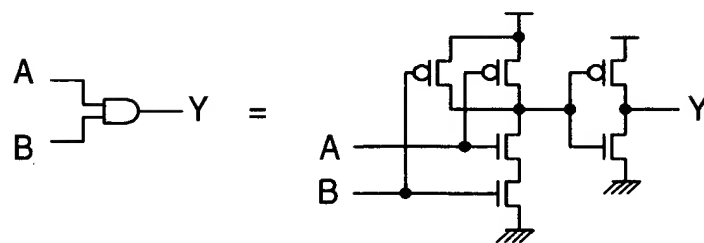


FIG.10

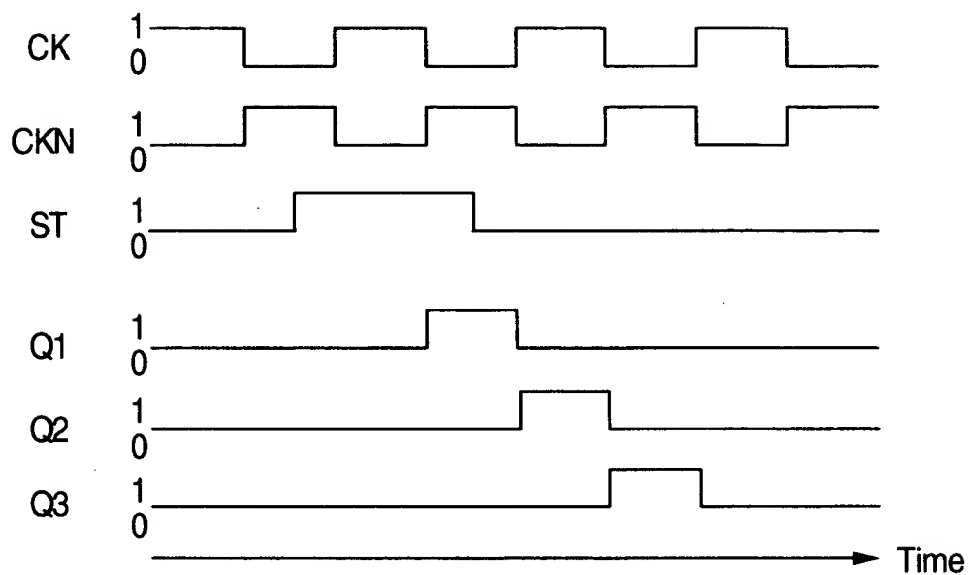


FIG.11

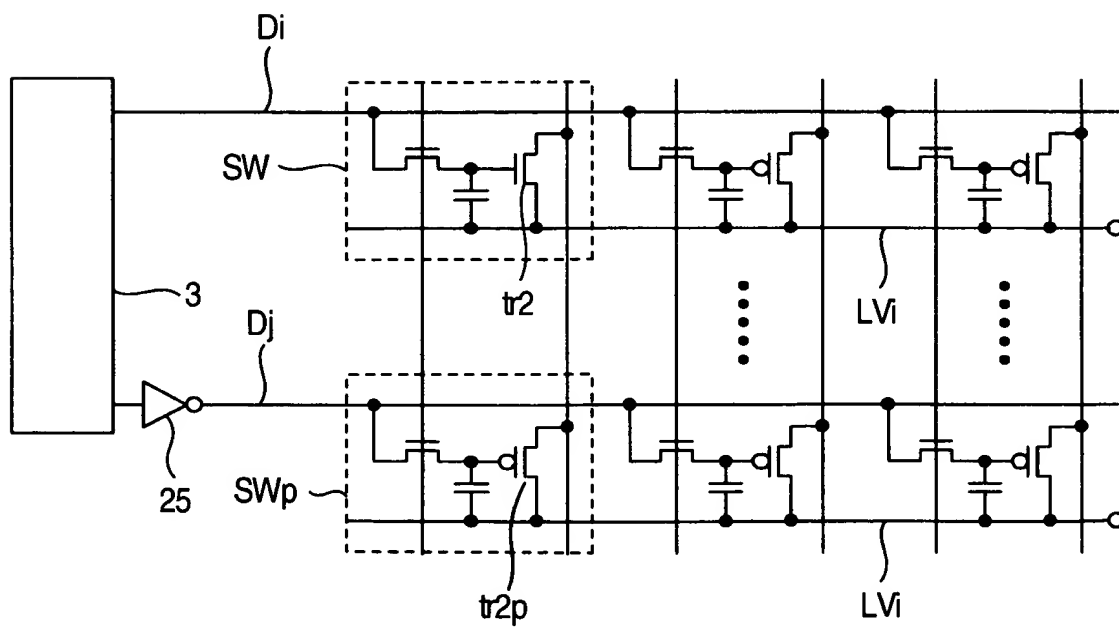


FIG.12

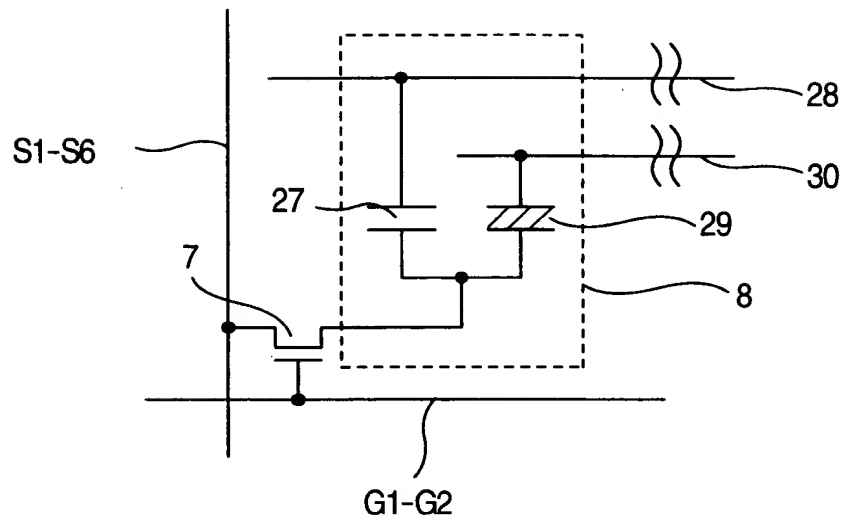


FIG.13

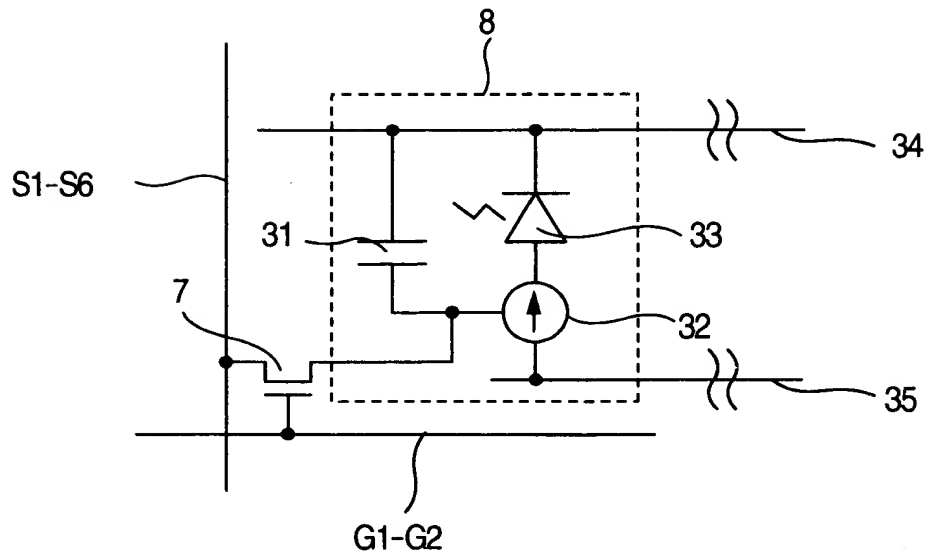
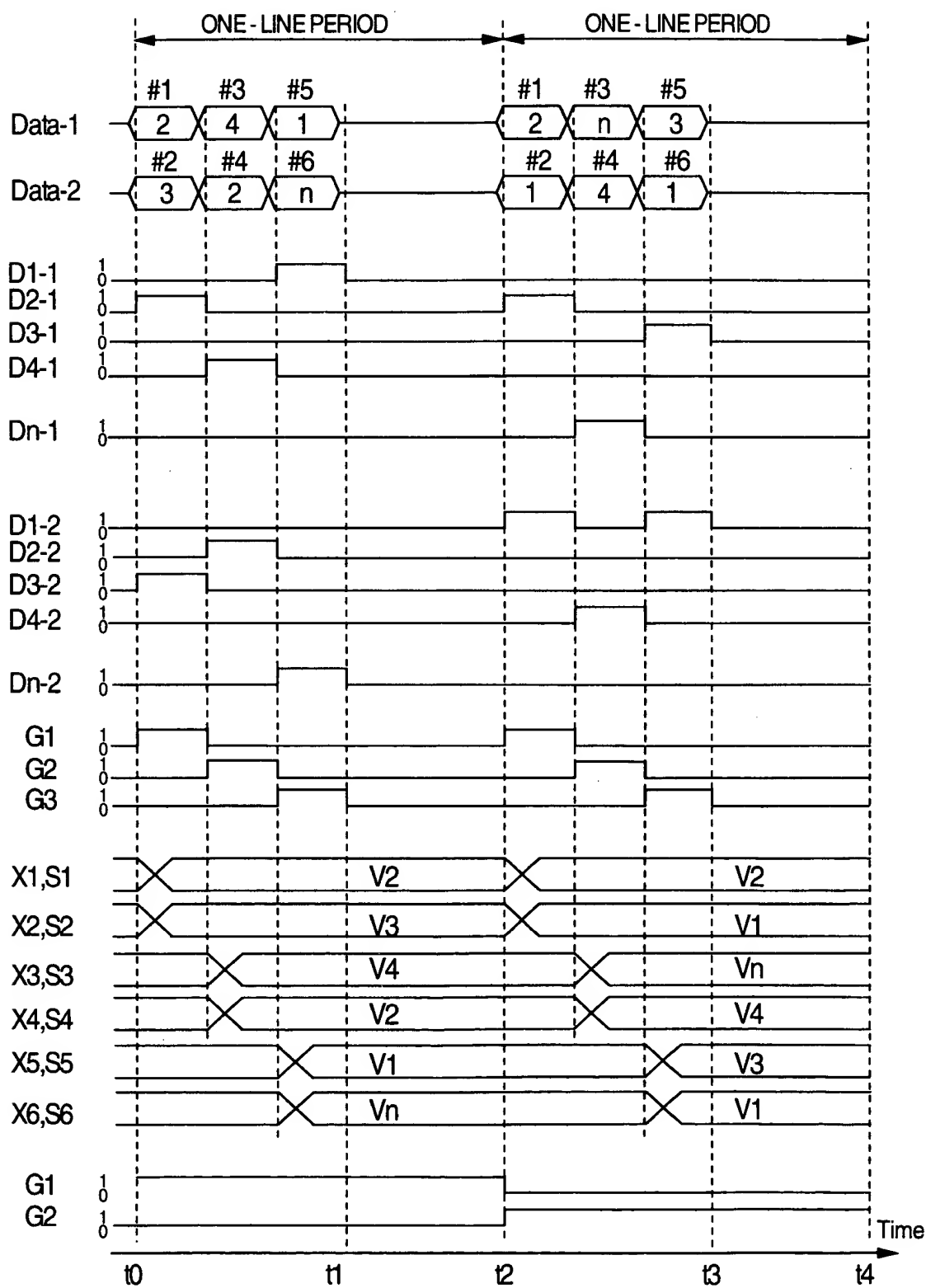


FIG.14



100230-ET2200

FIG.15

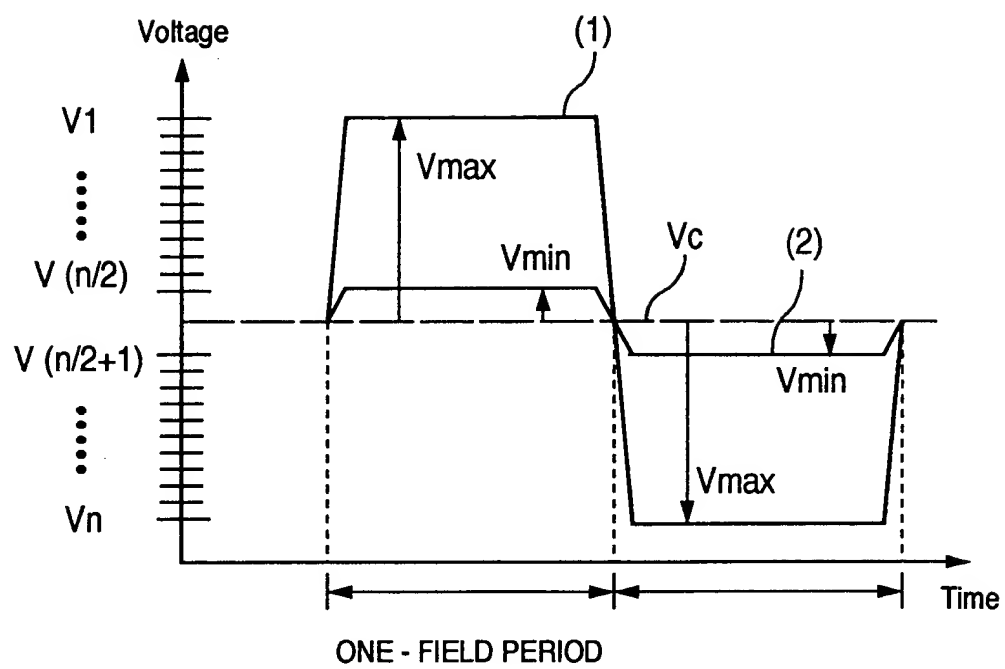


FIG.16

	in	out - 1	out - 2	out - 3	...	out - n	out - (n/2+1)	...	out - (n-2)	out - (n-1)	out - n
Odd	1	1	0	0	0	All 0				
	2	0	1	0	0					
	3	0	0	1	0					
					
	n/2	0	0	0	1					
Even	1	All 0					0	0	0	1
	2						0	0	1	0
	3						0	1	0	0

	n/2						1	0	0	0

FIG.17

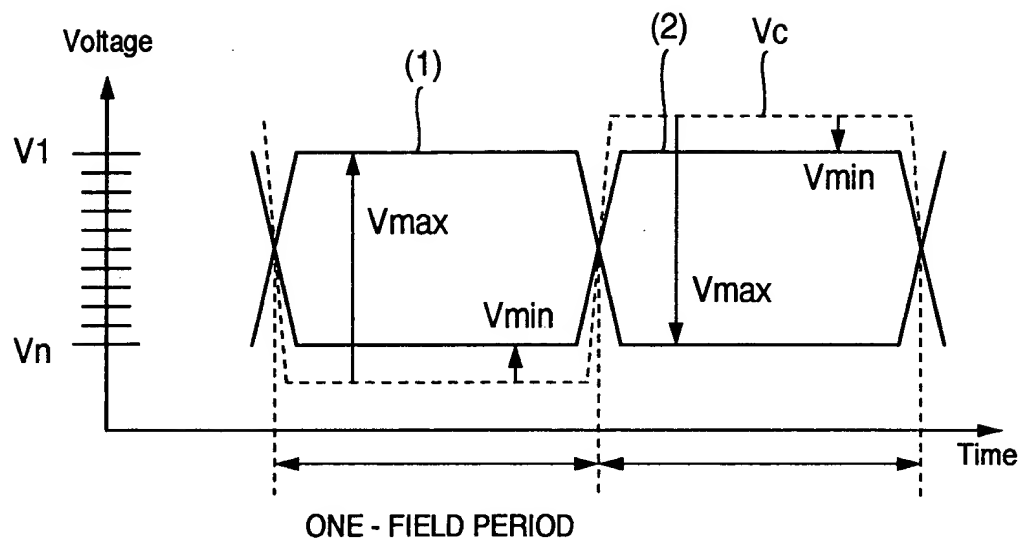


FIG.18

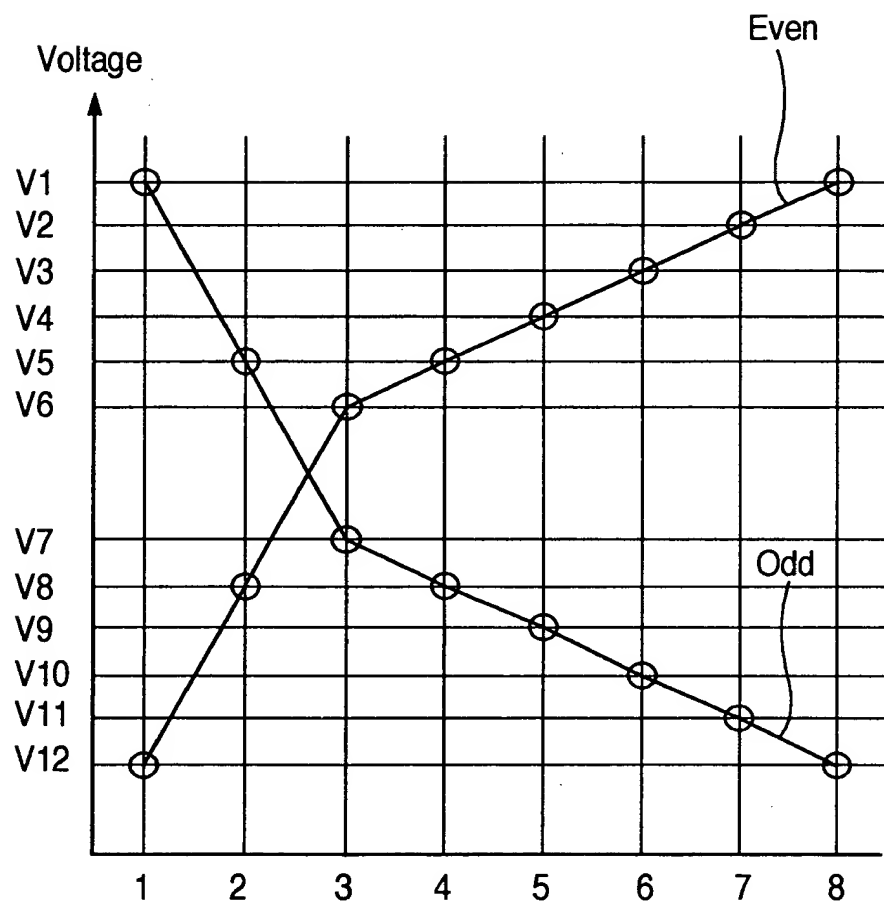


FIG.19

	in	out-1	out-2	out-3	out-4	out-5	out-6	out-7	out-8	out-9	out-10	out-11	out-12
Odd	1	1	0	0	0	0	0	0	0	0	0	0	0
	2	0	0	0	0	1	0	0	0	0	0	0	0
	3	0	0	0	0	0	0	1	0	0	0	0	0
	4	0	0	0	0	0	0	0	1	0	0	0	0
	5	0	0	0	0	0	0	0	0	1	0	0	0
	6	0	0	0	0	0	0	0	0	0	1	0	0
	7	0	0	0	0	0	0	0	0	0	0	1	0
	8	0	0	0	0	0	0	0	0	0	0	0	1
Even	1	0	0	0	0	0	0	0	0	0	0	0	1
	2	0	0	0	0	0	0	0	1	0	0	0	0
	3	0	0	0	0	0	1	0	0	0	0	0	0
	4	0	0	0	0	1	0	0	0	0	0	0	0
	5	0	0	0	1	0	0	0	0	0	0	0	0
	6	0	0	1	0	0	0	0	0	0	0	0	0
	7	0	1	0	0	0	0	0	0	0	0	0	0
	8	1	0	0	0	0	0	0	0	0	0	0	0

FIG. 19

FIG.20

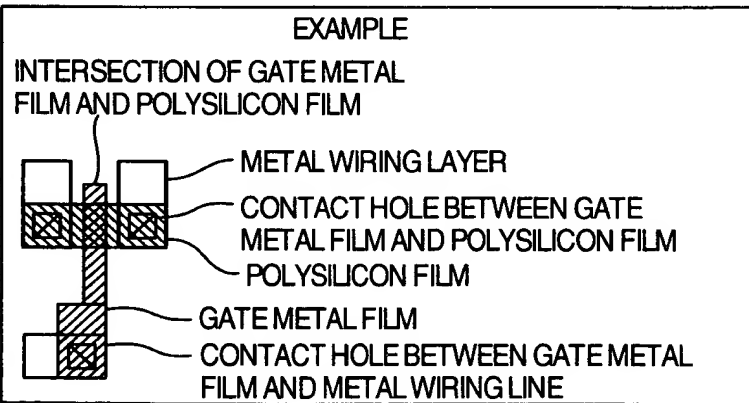
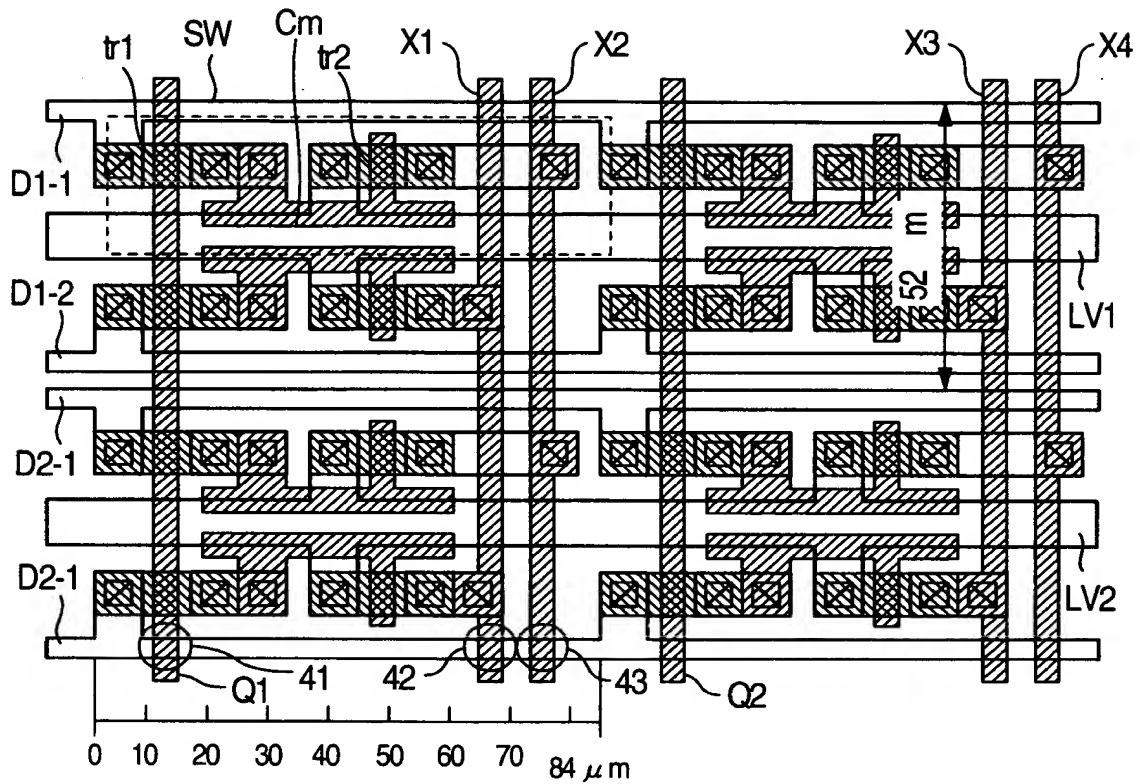


FIG.21

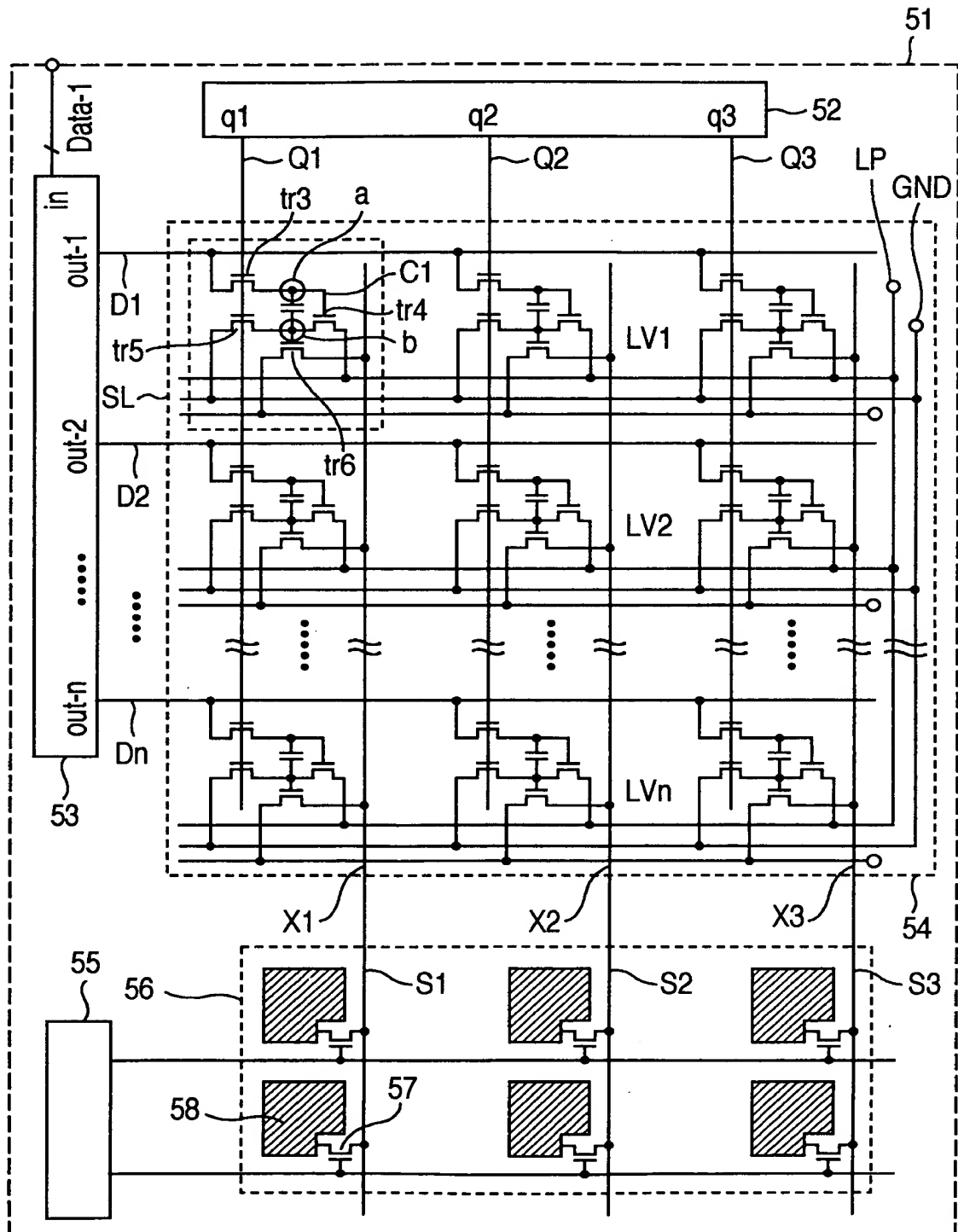


FIG.22

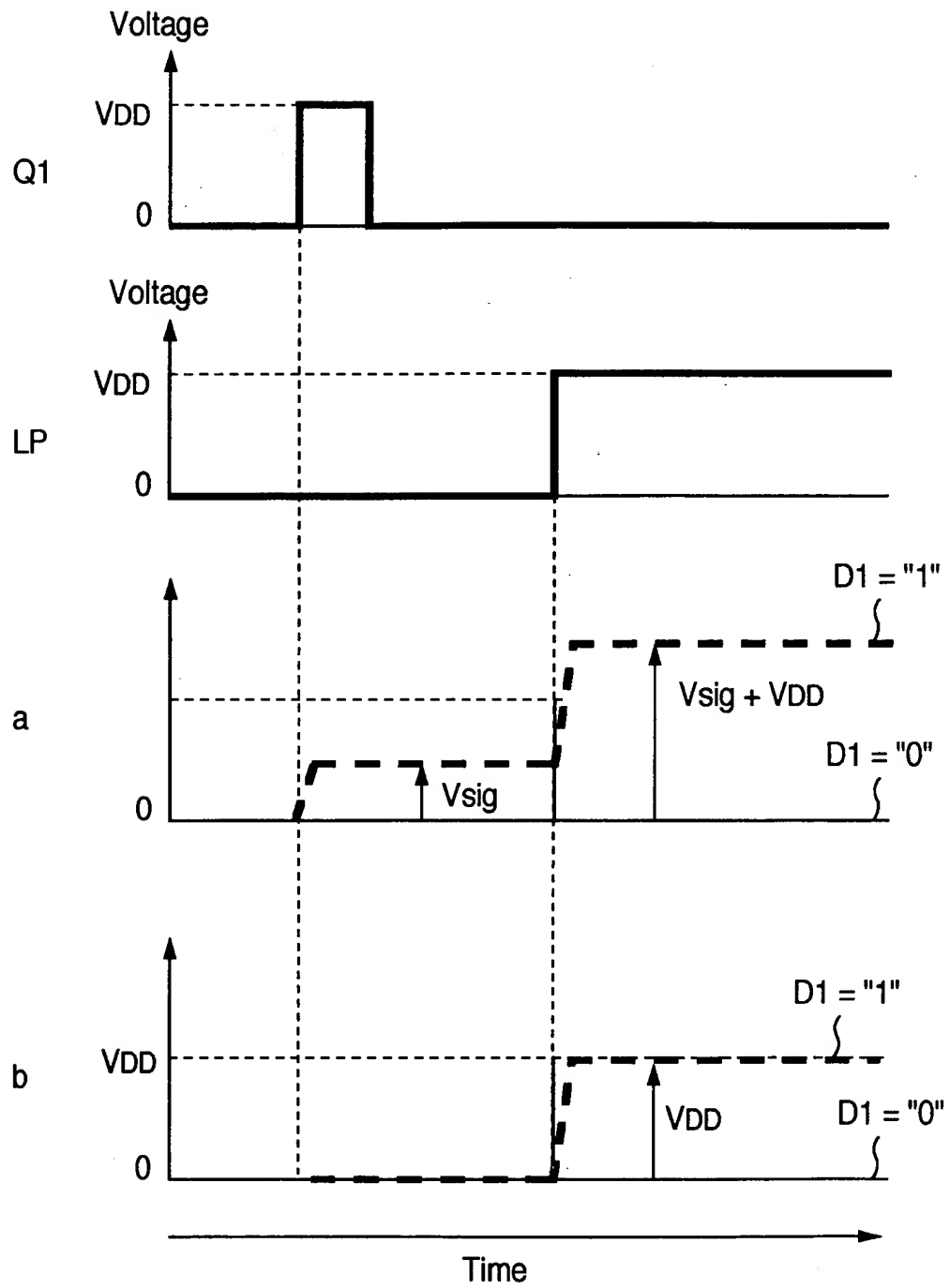


FIG. 22

FIG.23

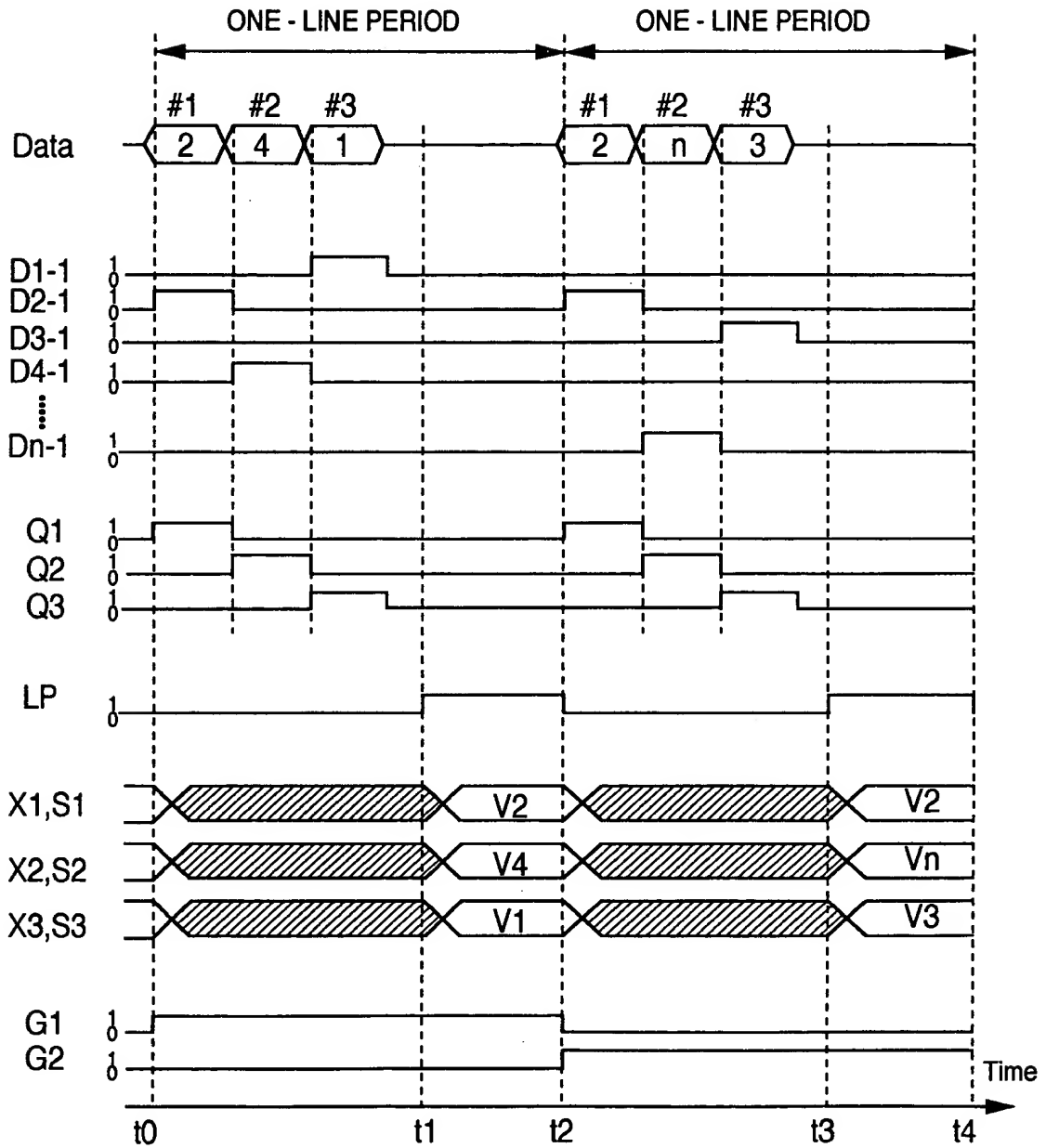


FIG.24

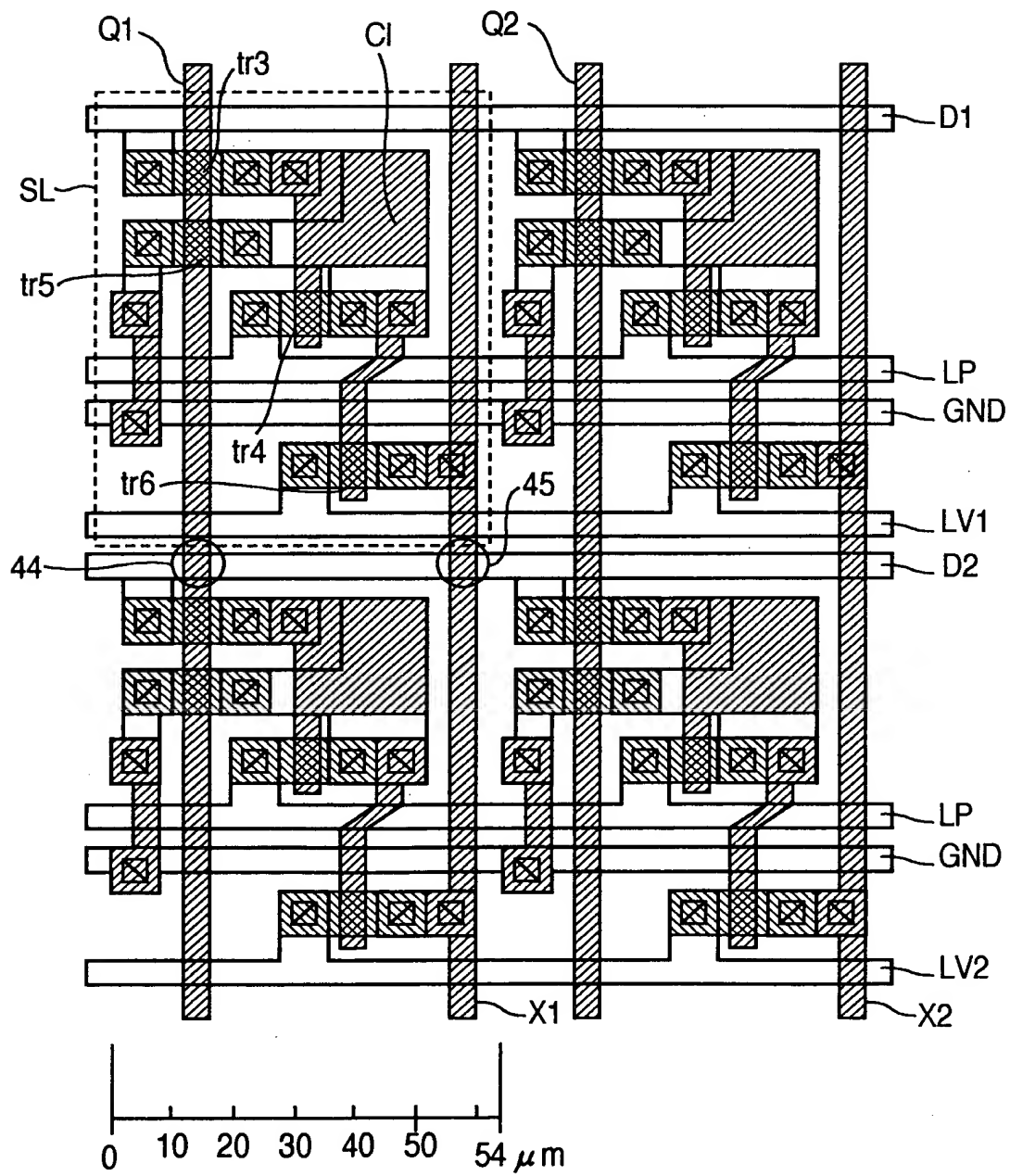


FIG.25

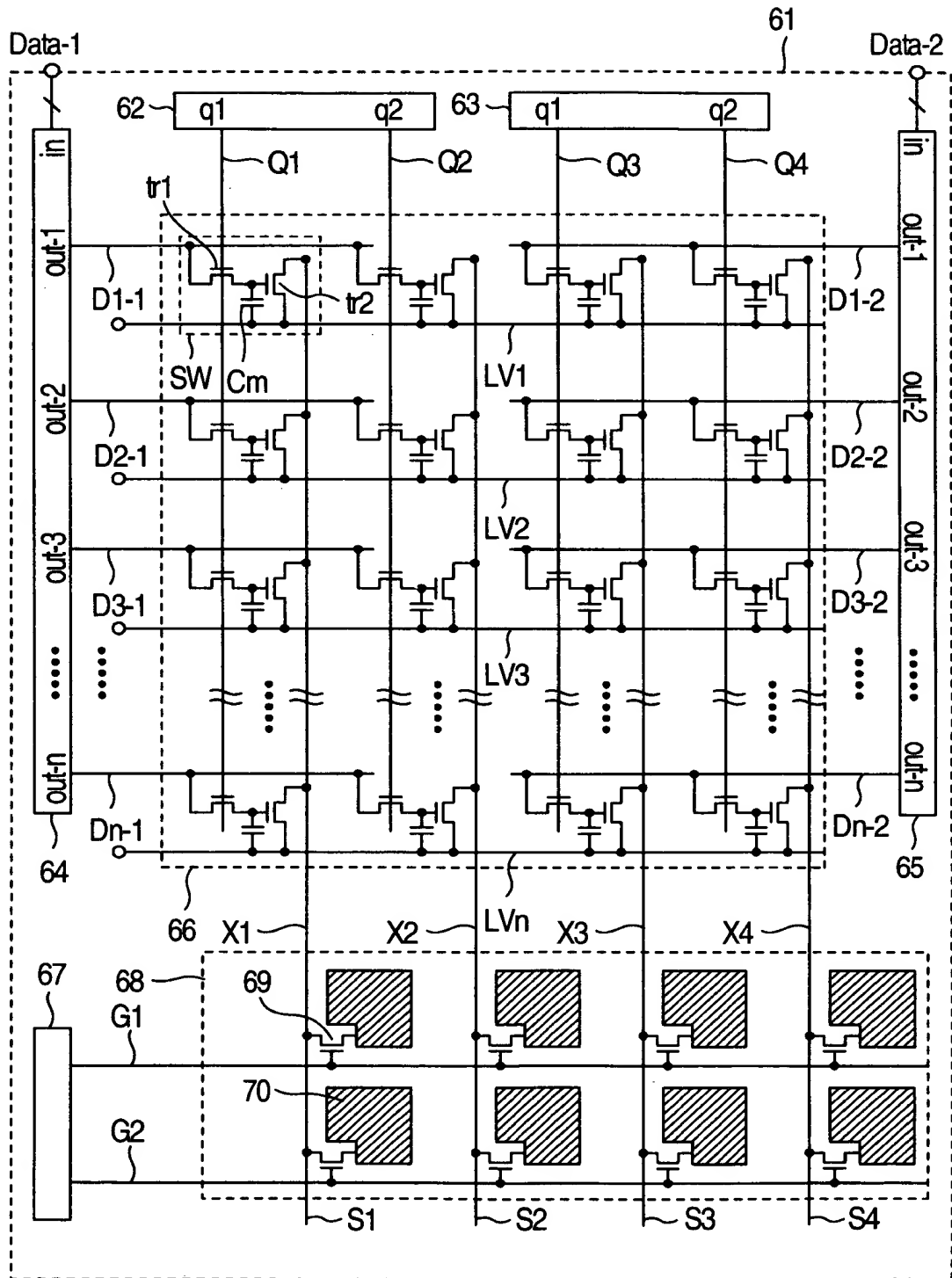


FIG.26

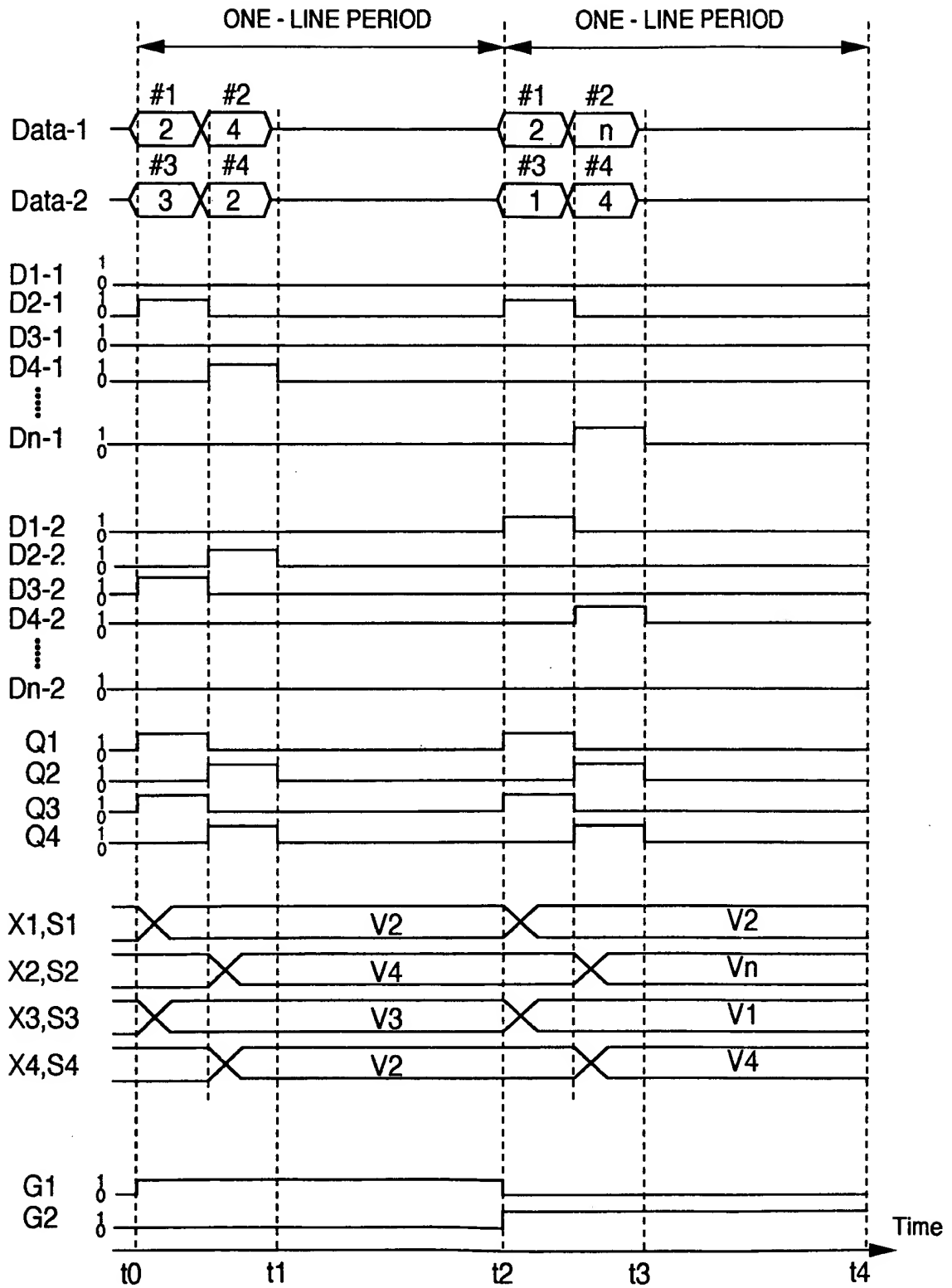


FIG.27

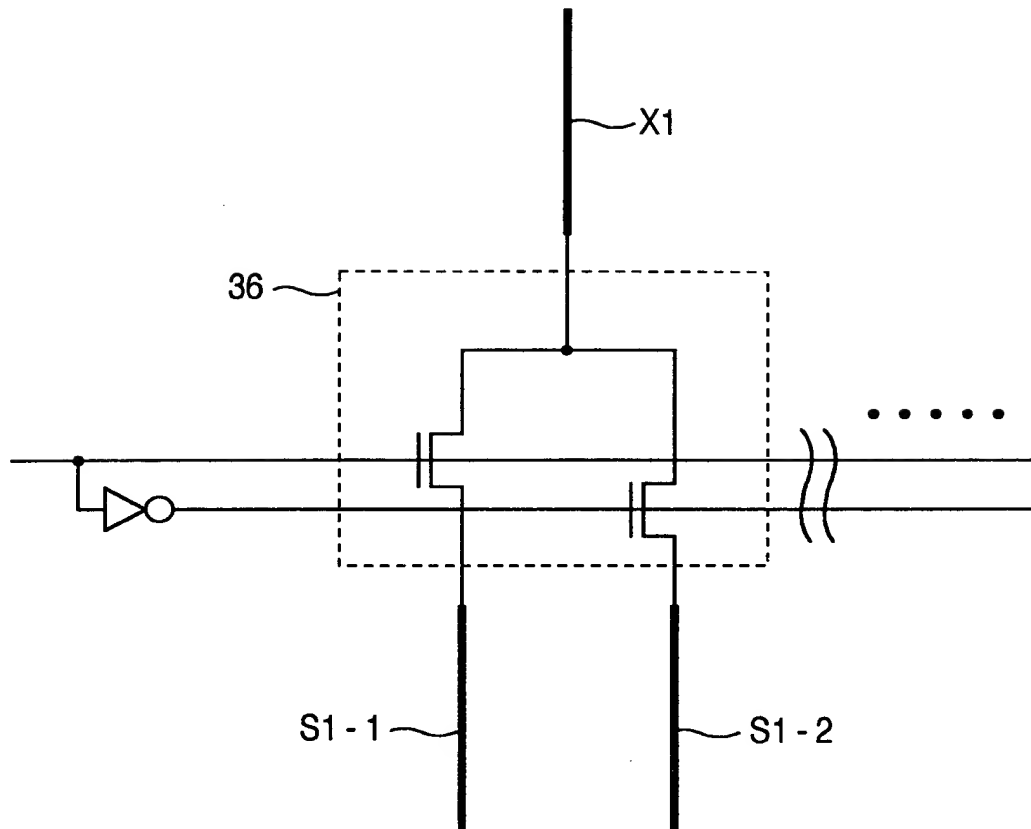


FIG. 27